CLAIMS

What is claimed is:

1   1.   An apparatus comprising:
2   a mask generator to generate a mask field for an operand having a word length,
3   the mask field defining an operand field within the operand to be operated by an
4   operation, the operand field having a field length; and
5   an execution unit coupled to the mask generator to execute the operation on the
6   operand field.

1   2.   The apparatus of claim 1 wherein the mask generator comprises:
2   a first decoder to decode a begin position specifier into a begin bit pattern;
3   a second decoder to decode an end position specifier into an end bit pattern; and
4   a logic circuit coupled to the first and second decoders to combine the begin and
5   end bit patterns into the mask field having the field length limited by the begin and end
6   positions.

1   3.   The apparatus of claim 1 wherein the execution unit comprises:
2   a field arithmetic logic unit (ALU) to generate an ALU result using one of an
3   arithmetic and logic operations on the operand field of at least one of first and second
4   ALU operands.

1   4.   The apparatus of claim 3 wherein the execution unit further comprises:
2   an operand selector to select a selector operand from a source operand and an
3   immediate operand, the source operand being from a register file.

1   5.   The apparatus of claim 4 wherein the execution unit further comprises:
2   a first barrel shifter coupled to the operand selector to shift the selector operand
3   to generate the first ALU operands according to one of the begin and end positions.

1   6.   The apparatus of claim 5 wherein the execution unit further comprises:
2   a second barrel shifter coupled to the field ALU to shift the ALU result.

1   7.   The apparatus of claim 5 wherein the execution unit further comprises:

2   a context selector coupled to the field ALU to select a field result, on a bit-by-

3 bit basis according to the operand field, from at least one of the first and second ALU

4 operands and the ALU result.

1   8.   The apparatus of claim 6 wherein the execution unit further comprises:

2   a context selector coupled to the field ALU to select a field result, on a bit-by-

3 bit basis according to the operand field, from at least one of the first and second ALU

4 operands, the ALU result, and the shifted ALU result.

1   9.   The apparatus of claim 3 wherein the field ALU comprises:

2   N single bit ALUs connected in cascade to generate the field result, the field

3 result including a single bit ALU result.

1   10.   The apparatus of claim 9 wherein the field result includes at least a

2 condition code representing a condition of the field result.

1   11.   The apparatus of claim 9 wherein the single bit ALU comprises:

2   an adder/ subtractor to perform an add/ subtraction on the first and second ALU

3 operands and generate a carry output.

1   12.   The apparatus of claim 11 wherein the single bit ALU further

2 comprising:

3   a zero section to generate a zero condition code using a carry from a less

4 significant section;

5   a negative section to generate a out sign bit for the field result using current and

6 next operand fields; and

7   an overflow section to generate an overflow bit for the field result using the next

8 operand field.

1   13.   The apparatus of claim 2 further comprising:

2   a field specifier selector coupled to the mask generator to generate at least one

3 of the begin and end position specifiers.

1   14.   The apparatus of claim 13 wherein the field specifier selector generates

2   the at least one of the begin and end position specifiers from at least one of an

3   instruction specifying the operation, a general-purpose register, a special-purpose

4   register, and a configuration register.

1   15.   The apparatus of claim 1 wherein the operand field is one of a

2   contiguous field and a non-contiguous field.

1   16.   A method comprising:

2   generating a mask field for an operand having a word length, the mask field

3   defining an operand field within the operand to be operated by an operation, the

4   operand field having a field length; and

5   executing the operation on the operand field, leaving portion outside the

6   operand field unchanged.

1   17.   The method of claim 16 wherein generating the mask field comprises:

2   decoding a begin position specifier into a begin bit pattern;

3   decoding an end position specifier into an end bit pattern; and

4   combining the begin and end bit patterns into the mask field having the field

5   length limited by the begin and end positions.

1   18.   The method of claim 16 wherein executing the operation comprises:

2   generating an ALU result using one of an arithmetic and logic operations on the

3   operand field of at least one of first and second ALU operands.

1   19.   The method of claim 18 wherein executing the operation further

2   comprises:

3   selecting a selector operand from a source operand and an immediate operand,

4   the source operand being from a register file.

1   20.   The method of claim 19 wherein executing the operation further

2   comprises:

3   shifting the selector operand to generate the first ALU operands according to

4 one of the begin and end positions.

1   21.   The method of claim 20 wherein executing the operation further

2 comprises:

3   shifting the ALU result.

1   22.   The method of claim 20 wherein executing the operation comprises:

2   selecting a field result, on a bit-by-bit basis according to the operand field, from

3 the first and second ALU operands and the ALU result.

1   23.   The method of claim 21 wherein executing the operation comprises:

2   selecting a field result, on a bit-by-bit basis according to the operand field, from

3 the first and second ALU operands, the ALU result, and the shifted ALU result.

1   24.   The method of claim 23 wherein generating the ALU result comprises:

2   generating the field result using N single bit ALUs connected in cascade, the

3 field result including a single bit ALU result.

1   25.   The method of claim 24 wherein the field result includes at least a

2 condition code representing a condition of the field result.

1   26.   The method of claim 24 wherein generating the field result comprises:

2   performing an add/ subtraction on the first and second ALU operands; and

3   generating a carry output.

1   27.   The method of claim 26 wherein generating the field result further

2 comprises:

3   generating a zero condition code using a carry from a less significant section;

4   generating a sign bit for the field result using current and next operand fields;

5 and

6   generating an overflow bit for the field result using the next operand field.

1   28.   The method of claim 17 further comprising:

2   generating at least one of the begin and end position specifiers using a field

3   specifier selector.

1   29.   The method of claim 28 wherein generating at least one of the begin and

2   end position specifiers comprises generating the at least one of the begin and end

3   position specifiers from at least one of an instruction specifying the operation, a

4   general-purpose register, a special-purpose register, and a configuration register.

1   30.   The method of claim 16 wherein the operand field is one of a contiguous

2   field and a non-contiguous field.

1   31.   A processor core comprising:

2   a register file having a plurality of registers;

3   a condition code register to store condition codes resulted from an operation;

4   and

5   a field processing unit coupled to the register file and the condition code register

6   to perform an operation, the field processing unit comprising:

7   a mask generator to generate a mask field for an operand having a word

8   length, the mask field defining an operand field within the operand to be operated by

9   the operation, the operand field having a field length, and

10   an execution unit coupled to the mask generator to execute the operation

11   on the operand field, leaving portion outside the operand field unchanged.

1   32.   The processor core of claim 31 wherein the mask generator comprises:

2   a first decoder to decode a begin position specifier into a begin bit pattern;

3   a second decoder to decode an end position specifier into an end bit pattern; and

4   a logic circuit coupled to the first and second decoders to combine the begin and

5   end bit patterns into the mask field having the field length limited by the begin and end

6   positions.

1   33.   The processor core of claim 31 wherein the execution unit comprises:

2   a field arithmetic logic unit (ALU) to generate an ALU result using one of an

3   arithmetic and logic operations on the operand field of at least one of first and second

4   ALU operands.

1   34.   The processor core of claim 33 wherein the execution unit further

2   comprises:

3   an operand selector to select a selector operand from a source operand and an

4   immediate operand, the source operand being from a register file.

1   35.   The processor core of claim 34 wherein the execution unit further

2   comprises:

3   a first barrel shifter coupled to the operand selector to shift the selector operand

4   to generate the first ALU operands according to one of the begin and end positions.

1   36.   The processor core of claim 34 wherein the execution unit further

2   comprises:

3   a second barrel shifter coupled to the operand selector to shift the ALU result.

1   37.   The processor core of claim 35 wherein the execution unit further

2   comprises:

3   a context selector coupled to the field ALU to select a field result, on a bit-by-

4   bit basis according to the operand field, from at least one of the first and second ALU

5   operands and the ALU result.

1   38.   The processor core of claim 36 wherein the execution unit further

2   comprises:

3   a context selector coupled to the field ALU to select a field result, on a bit-by-

4   bit basis according to the operand field, from at least one of the first and second ALU

5   operands, the ALU result, and the shifted ALU result.

1   39.   The processor core of claim 36 wherein the field ALU comprises:

2   N single bit ALUs connected in cascade to generate the field result, the field

3   result including a single bit ALU result.

1   40.   The processor core of claim 39 wherein the field result includes at least

2   a condition code representing a condition of the field result.

1   41.   The processor core of claim 39 wherein the single bit ALU comprises:

2   an adder/ subtractor to perform an add/ subtraction on the first and second ALU

3   operands and generate a carry output.

1   42.   The processor core of claim 41 wherein the single bit ALU further

2   comprising:

3   a zero section to generate a zero condition code using a carry from a less

4   significant section;

5   a negative section to generate a out sign bit for the field result using current and

6   next operand fields; and

7   an overflow section to generate an overflow bit for the field result using the next

8   operand field.

1   43.   The processor core of claim 32 wherein the field processing unit further

2   comprises:

3   a field specifier selector coupled to the mask generator to generate at least one

4   of the begin and end position specifiers.

1   44.   The processor core of claim 43 wherein the field specifier selector

2   generates the at least one of the begin and end position specifiers from at least one of an

3   instruction specifying the operation, a general-purpose register, a special-purpose

4   register, and a configuration register.

1   45.   The processor core of claim 31 wherein the operand field is one of a

2   contiguous field and a non-contiguous field.